BOSE INSTITUTE KOLKATA	
Tender No.	CAPSS/86/241/CBM-MUCH-SKG)/2016-17
Tender Date	24.10.2016
Tender Type	OPEN
Tender Title	NAT-JSM-00
Specification	Please see Annexure - 1
Quantity	01
Last Date & Time for submission	15.11.2016 upto 13:00 hrs.
Date & Time for opening bids	15.11.2016 at 15:00 hrs.
Submission of Tender (address)	CAPSS, Bose Institute, Kolkata 700 091
Venue of bid opening	CAPSS, Bose Institute, Kolkata 700 091
For any query the interested bidders may contact (Dept./Section/Div./Unit)	033 2569 3123 / 28 /29
General Terms & Conditions	
Warranty	365 days from the date of satisfactory commissioning
Payment terms	Payment will be made after complete delivery of the instrument in good condition and satisfactory installation
Delivery schedule	Within 45 days from the date of order & if any defect of the supplied item is found, it should be replaced immediately from your side
Bid security (earnest money deposit) if applicable	NA
Submission of Performance Bank Guarantee (PBG), if applicable	NA
Any other information (if applicable)	NA
Name of the instrument and submission of tender should be mentioned on the envelop positively	
Director, Bose Institute reserves the right to accept or reject any or all tenders either in part or in full. The reasons of rejecting the tender of a prospective bidder will be disclosed only when enquiries are made	

Sr. Prof. & Incharge, Registrar's Office

Annexure – 1

Detailed Technical specifications

- JTAG download via MCH through Ethernet
- JTAG programming connector at front panel
- Automatic arbitration between JTAG Masters
- Target selection through JTAG information
- Overrule of automatic operation and dedicated selection of JTAG target by front panel elements
- Multiple JSM pinout configurations via FPGA

Physical Dimemsions

- Single-width AMC module: width 73.5 mm (2.89 in), depth: 180.6 mm (7.11 in)

Subsystem Processor

- Altera Cyclone® III FPGA

Interface: Backplane

- TCP/IP: Protocol as used by the Xilinx Vivado or ISE design suites supports the XVC protocol, which allows JTAG commands to pass over IP to an embedded system so that a target Xilinx FPGA can be programmed and/or debugged. The NAT-MCH parses the IP packets with a TCP/IP connection and converts the packets into JTAG commands. After the packets are processed, the NAT-MCH communicates with the NAT-JSM over an internal protocol. The NAT-JSM switches the connection to the target device and provides logical connection between the XVC server and the target FPGA.

Interfaces: Front panel

- JTAG Header: The NAT-JSM provides a XILINX compatible 14-pin programming header on the front panel. With a standard XILINX programming adapter, you can program or debug the resources in a MTCA system. The Interface has been tested successfully with the Xilinx Platform Cable USB II. You select the programming target using the rotary switch on the front panel or through the web interface of the NAT-MCH.
- Mini USB: A mini USB connector on the front panel provides a direct connection to the on-board USB-to-JTAG bridge for common programming adapters from various vendors. To use this programming interface, the software driver of the respective tool should support programming interfaces based on the FTDI FT2232 USB-to-JTAG chip. The interface has been tested successfully with Lattice Diamond Programmer 3.0. You select the programming target using the rotary switch on the front panel or through the web interface of the NAT-MCH.

Environmental Conditions

- Temperature (operating): 0ºC to +50ºC with forced air cooling
- Temperature (storage):-40ºC to +85ºC
- Relative Humidity:10% to 90% at +55ºC (non-condensing)

Power Consumption

Power is to be supplied through the backplane connector, the onboard power converter has a range from +5V to +12V. Current draw is not more than 200mA.