

BOSE INSTITUTE  
KOLKATA

Tender No.	<b>CAPSS/15/37(ALICE-SD)/13-14</b>
Tender Date	<b>15/07/2013</b>
Tender Type	<b>OPEN</b>

Tender Title	<b>FPGA Design Suite</b>
Specification	<ul style="list-style-type: none"> <li>• Xilinx ISE Design Suite 14.4 or Higher (System Edition) with at least 25 user' licence</li> <li>• ISE foundation tools with ISE Simulator (ISIM)</li> <li>• ChipScore Pro Logic analyzer</li> <li>• ChipScore Pro Serial I/O toolkit</li> <li>• Embedded development kit (EDK)</li> <li>• Software development kit (SDK)</li> <li>• System generator for DSP</li> <li>• Device support for : Xilinx Virtex-7 to Virtex-4 FPGAs Xilinx Kintex-7 FPGAs</li> <li>• CoolRunner XPLA3, CoolRunner - II, CoolRunner-IIA CPLDs</li> </ul>
Quantity	<b>ONE</b>

Last Date & Time for submission	31/07/2013 upto 2.00 pm
Date & Time for opening bids	31/07/2013 at 3:00 p.m.
Submission of Tender (address)	CAPSS, Salt Lake, Block EN 80, Kolkata 700 091
Venue of bid opening	CAPSS, Salt Lake, Block EN 80, Kolkata 700 091
For any query the interested bidders may contact (Dept./Section/Div./Unit)	033 2569 3109/3123

<b>General Terms &amp; Conditions</b>
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Warranty	12 months from date of satisfactory installation
Payment terms	Payment will be made after complete delivery of the instrument in good condition and satisfactorily installation.
Delivery schedule	Within 30 days from the date of receiving order & if any defect of the supplied item is found, it should be replaced immediately from your side.

Bid security (earnest money deposit) if applicable	N.A.
Submission of Performance Bank Guarantee (PBG), if applicable	N.A.
Any other information (if applicable)	

*Name of the instrument and submission of tender should be mentioned on the envelop positively*

**Director, Bose Institute reserves the right to accept or reject any or all tenders either in part or in full. The reasons for rejecting the tender of a prospective bidder will be disclosed only when enquiries are made.**

Registrar  
16.7.2013